ABSTRACT OF THE INVENTION

A process for forming copper metal interconnects and copper-filled vias in a dielectric layer on an integrated circuit structure wherein the impurity level of the copper-filled metal lines and copper-filled vias is lowered, resulting in an increase in the average grain size of the copper, a reduction of the resistivity, and more homogeneous distribution of the stresses related to the formation of the copper metal lines and copper-filled vias throughout the deposited copper. The process comprises: depositing a partial layer of copper metal in trenches and via openings previously formed in one or more dielectric layers, then annealing the deposited copper layer at an elevated temperature for a predetermined period of time; and then repeating both the deposit step and the step of annealing the deposited layer of copper one or more additional times until the desired final thickness is reached. After the deposition and annealing of the deposited copper, the annealed structure is then planarized preferably using, for example, a chemical mechanical polishing (CMP) process, and then the planarized structure is again annealed. Preferably the process further includes removing a thin portion of copper from the surface of the deposited and annealed copper layer.